AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. The following listing provides the amended claims with the amendments marked with deleted material crossed out and new material underlined to show the changes made.

Claims 1-57 (Canceled)

58. (Previously presented) A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a plurality of nets each of which includes a plurality of circuit elements in the IC layout, wherein the computer program uses a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets, said wiring model having diagonal lines, the computer program comprising sets of instructions for:

a) defining, for each particular net, a minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net, said minimum spanning trees having edges, wherein at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal,

b) calculating the length of the edges of the minimum spanning trees; and

c) combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets.

59. (Previously presented) The computer readable medium of claim 58, wherein some of the diagonal edges are in the same direction as some of the diagonal

lines in the wiring model.

60. (Previously presented) The computer readable medium of claim 58, wherein the computer program further comprises sets of instructions for:

a) moving a circuit element from a first location in the IC layout to a second location in this layout;

b) defining, for each net containing the moved circuit element, a new minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net after the move, said minimum spanning trees having edges, wherein at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal,

c) calculating the length of the new minimum spanning trees to estimate the change in the total interconnect-line length.

61. (Previously presented) A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a plurality of nets each of which includes a plurality of circuit elements in the IC layout, wherein the computer program uses a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets, said wiring model having diagonal lines, the computer program comprising sets of instructions:

a) defining, for each particular net, a Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net, said Steiner trees having edges, wherein at least one of the edges of at least one of the Steiner trees is

at least partially diagonal;

b) calculating the length of the Steiner trees; and

c) combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets.

62. (Previously presented) The computer readable medium of claim 61, wherein some of the diagonal edges are in the same direction as some of the diagonal lines in the wiring model.

63. (Previously presented) The computer readable medium of claim 61, wherein the computer program further comprises a set of instructions for defining a set of Steiner points for at least some of the nets.

64. (Previously presented) The computer readable medium of claim 61, wherein the computer program further comprises sets of instructions for:

a) moving a circuit element from a first location in the IC layout to a second location in this layout;

b) for each net containing the moved circuit element, defining a new Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net after the move, said new Steiner trees having edges, wherein at least one of the edges of at least one of the new Steiner trees is at least partially diagonal,

c) calculating the length of the new Steiner trees to estimate the change in the total interconnect-line length.

Claims 65-96 (Canceled).